REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 10-18 remain pending. Claims 10-18 have been rejected.

Claims 10, 13, and 16 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 10, 12, 13, 15, 16 and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,021,483 to Ajanovic, et al. in view of U.S. Patent No. 5,948,084 to Solomon, et al. ("Solomon").

Applicants submit that the Examiner inadvertently referred to U.S. Patent No. 6,021,483 as the patent to Ajanovic, et al. In fact, U.S. Patent No. 6,021,483 is issued to Adar et al. The references in U.S. Patent No. 6,021,483 do not correspond to the references made by the Examiner in the Office Action dated 04/27/06.

Applicants submit that the Examiner meant to refer to the U.S. Patent No. 5,761,444 to Ajanovic, et al.

Therefore, Applicants in this response discuss the U.S. Patent No. 5,761,444 to Ajanovic, et al. (hereinafter "Ajanovic").

Claim 10 reads as follows:

> A method, comprising:
> dispatching a bus transaction from a requestor to a device;
> starting a timer in response to dispatching of the bus transaction;
> determining if the timer expires before the device responds to the dispatched bus transaction; and
> issuing a deferred transaction response to the requestor if the timer expires.

The Examiner acknowledged that Ajanovic does not disclose "starting a timer in response to dispatching of the bus transaction" (Office Action, 04/27/06, p. 2).

Ajanovic discloses deferring a current transaction when a new transaction is pending (Abstract). More specifically, Ajanovic discloses that the timer starts when the new transaction is waiting on the bus. The timer records the waiting time of the new pending transaction. Further, Ajanovic discloses determining the amount of the waiting time for the new pending transaction (col. 5, lines 24-31). In particular, Ajanovic discloses that if the timer exceeds the predetermined waiting time for the new pending transaction, the current transaction is deferred (col. 5, lines 32-55).

It is submitted that Ajanovic teaches away from the presently claimed invention. Ajanovic teaches deferring the current transaction if a predetermined time transpires (as determined by a timer), where the predetermined time is started from the time another transaction becomes available for issuance onto the bus. In contrast, claim 10 refers to issuing a deferred transaction response in response to a transaction after a different predetermined time transpires (as determined by a timer), where the predetermined time starts from the time the transaction itself issues, such that it is independent of any subsequent transaction that becomes ready for issuance.

Solomon discloses executing multiple transactions within a single arbitration cycle. More specifically, Solomon discloses starting a timer when the first transaction is executed. In particular, Solomon discloses that if the timer has not expired after the first transaction has been executed, another request for additional transaction from the same agent is granted (Figure 3, col. 6, lines 21-col. 7, line 5).

It is submitted that Solomon teaches away from the presently claimed invention. Solomon teaches adding the second transaction if the timer has not expired after execution of the first transaction. In contrast, claim 1 refers to issuing a deferred transaction response for a dispatched bus transaction if the timer expires before the device responds to this dispatched bus transaction.

Thus, Solomon, similarly to Ajanovic, fails to disclose, teach, or suggest issuing a deferred transaction response for a dispatched bus transaction if the timer expires before the device responds to the dispatched bus transaction, as recited in claim 10.

Applicants respectfully submit that Ajanovic does not teach or suggest a combination with Solomon, and Solomon does not teach or suggest a combination with Ajanovic. In fact, Ajanovic and Solomon teach away from one another. Ajanovic teaches deferring a current transaction in a presence of a new pending transaction to execute a single transaction at a time. Solomon, in contrast, teaches executing multiple transactions within a single arbitration cycle. It would be impermissible hindsight, based on Applicants' own disclosure, to combine Solomon and Ajanovic.

Furthermore, even if Solomon and Ajanovic were combined, such a combination would lack the following limitations of claim 10: issuing a deferred transaction response for a dispatched bus transaction to the requestor if the timer expires before the device responds to the dispatched bus transaction.

Therefore, Applicants respectfully submit that claim 10 is not obvious under 35 U.S.C. § 103(a) over Ajanovic in view of Solomon.

Because claims 12, 13, 15, 16 and 18 contain related limitations, Applicants respectfully submit that claims 12, 13, 15, 16 and 18 are not obvious under 35 U.S.C. § 103(a) over Ajanovic in view of Solomon.

Claims 11, 14 and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Ajanovic, in view of Solomon and further in view of U.S. Patent No. 5,493,566 to Ljungberg, et al ("Ljungberg").

Ljungberg discloses controlling of the flow of data cells through a packet switch. The packet switch has input and output buffers. The fullness of the output buffers is monitored and reported to an access device on the input side of the switch to stop the flow of data cells and hold them in the input buffers, when the fullness of the output buffers exceeds a predetermined level (Abstract).

It is respectfully submitted that Ajanovic does not teach or suggest a combination with Solomon and Ljungberg, Solomon does not teach or suggest a combination with Ajanovic and Ljungberg, and Ljungberg does not teach or suggest a combination with Ajanovic and Solomon. Ajanovic teaches deferring a current transaction in a presence of a new pending transaction to

execute a single transaction at a time. Solomon, in contrast, teaches executing multiple transactions within a single arbitration cycle. Ljungberg, in contrast to Ajanovic and Solomon, teaches a packet switch with input and output buffers to control the flow of data packets.

It would be impermissible hindsight, based on Applicants' own disclosure, to combine Ajanovic, Solomon, and Ljungberg.

Furthermore, even if Ajanovic, Solomon, and Ljungberg were combined, such a combination would lack the following limitations of claim 10: issuing a deferred transaction response for a dispatched bus transaction to the requestor if the timer expires before the device responds to the dispatched bus transaction.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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By: _____

Tatiana Rossin
Reg. No.: 56,833

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300